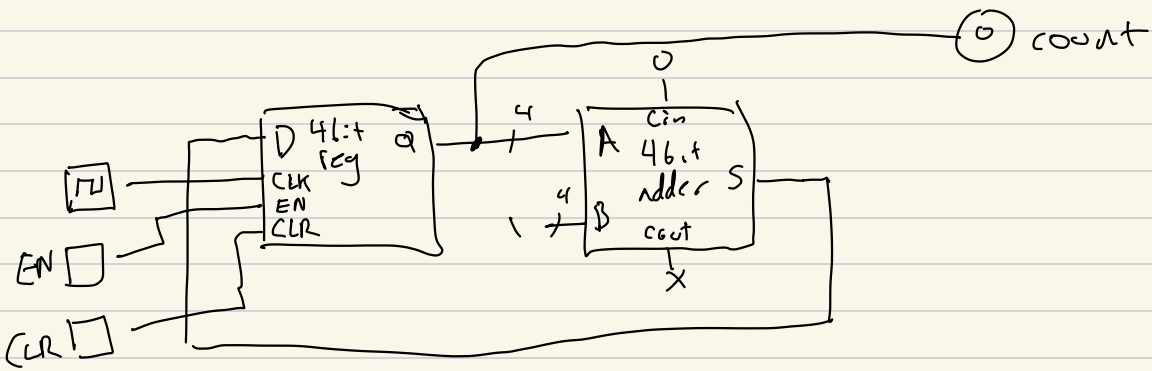
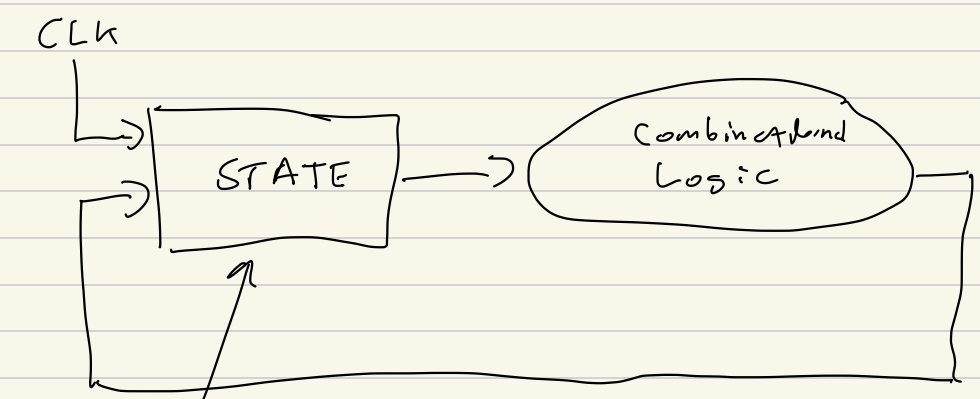
CS 631-01 Processor Design Components 2026-04-09

Combinational Logic → gates, sum-of-products
Sequential Logic → latches, D flipflop, resister
Clock, Multiplexor

Counter 4-bit Counter



Processor



Resisters x0-x31 | PC | Data Memory

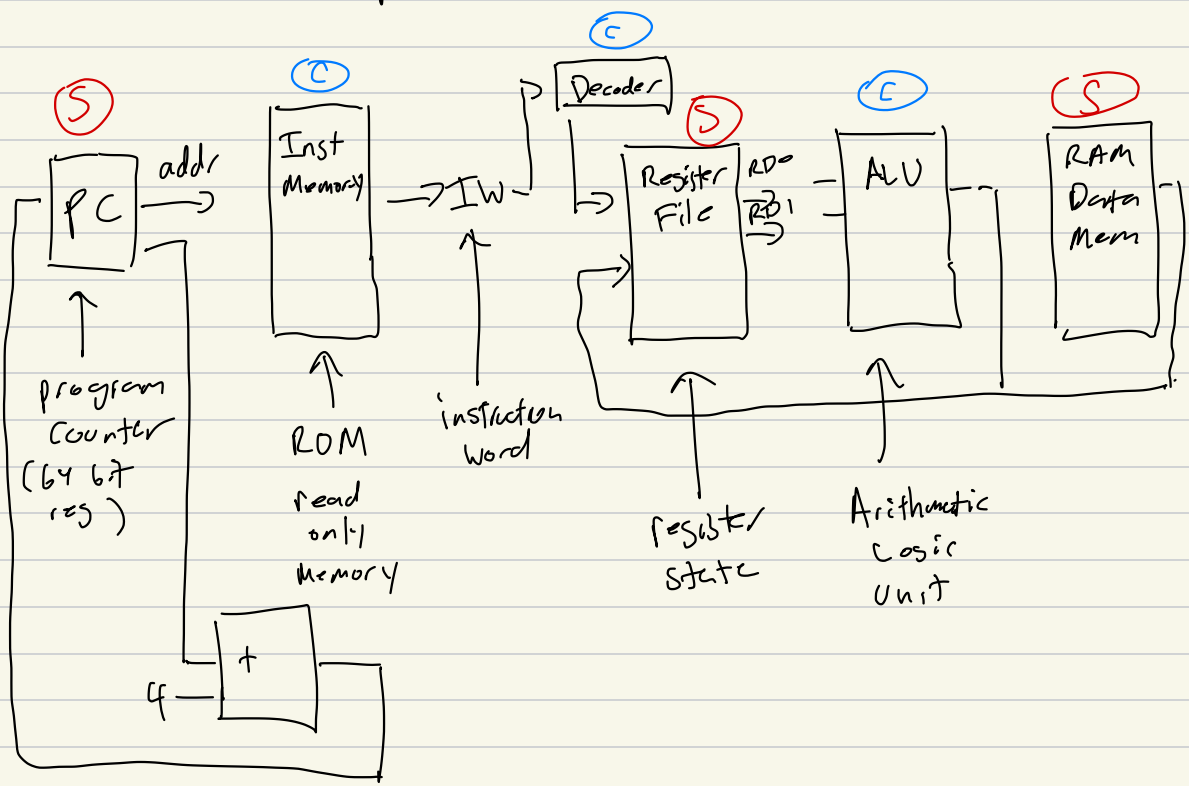
add t0, t1, t2

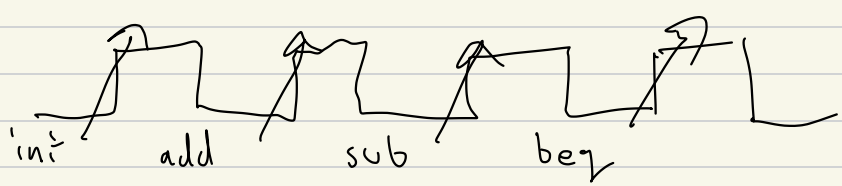
↑

rd

pc = pc + 4

Processor Components





single-cycle processor

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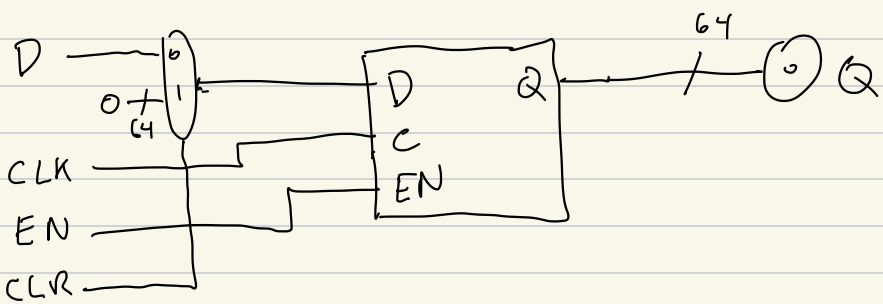
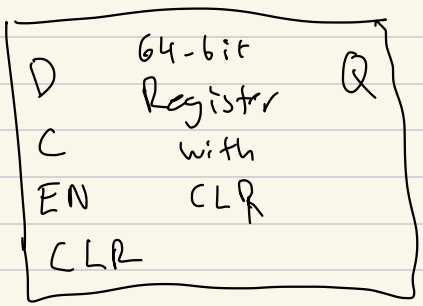
multi-cycle processor

↓

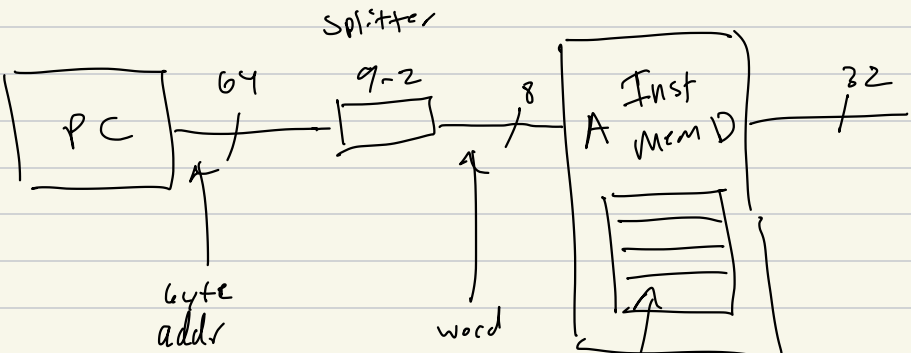
pipelined processor

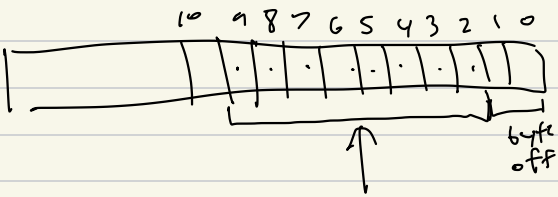
PC Program Counter



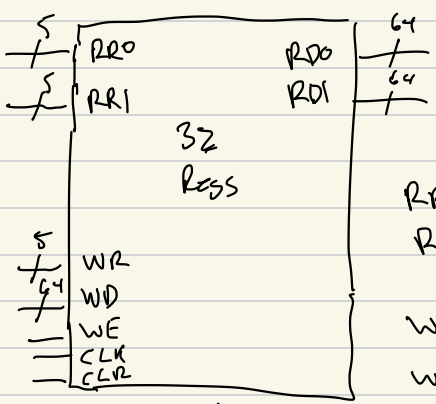


Instruction Memory





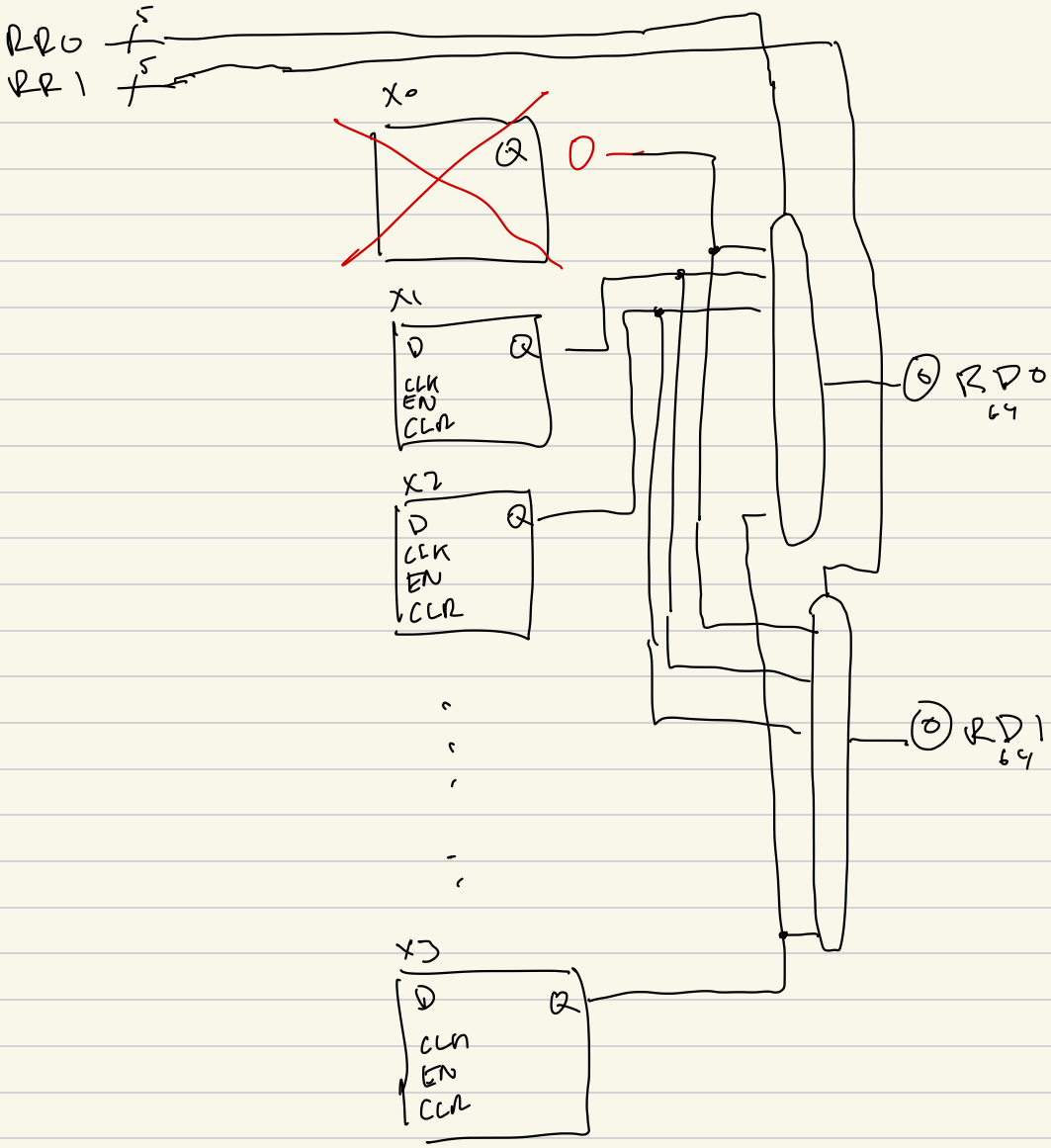
Register File



RR - read reg #
RD - read data value

WR - write register
WD - write data
WE - write enable

on a single clock cycle:
1) read up to two reg values
2) write at most to one register


RR0
5
RR1
5
X0
Q
0
X1
D
Q
CLK
EN
CLR
X2
D
Q
CLK
EN
CLR
X3
D
Q
CLK
EN
CLR
0
RD0
64
0
RD1
64